



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Edward Y. CHANG et. al.  
Serial No: 10/699,839  
Filed: November 4, 2003  
For: Growth of GaAs Epitaxial Layers On Si Substrate By Using  
A Novel GeSi Buffer Layer  
Atty Dkt: CHAN3228/EM

Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to Rule 37 C.F.R. §1.51(b), §1.56, §1.97, and §1.98, this Information Disclosure Statement is submitted in the above-identified patent application. A listing of documents to be published on the face of any patent granted from this application is submitted herewith on Form PTO-1449. Any other documents or information submitted for consideration by the Examiner are listed in this paper.

This Information Disclosure Statement is submitted prior to the mailing date of the first Office Action on the merits received by Applicant in the above identified application.

The Examiner is requested to acknowledge consideration of the information provided in this paper in accordance with prescribed procedures.

Please charge any additional fees or credit any overpayments in connection with this paper to Deposit Account No. 02-0200.

Respectfully submitted,

  
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Date: March 31, 2004

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| B/O Form PTO-1449<br><br>U.S. Department of Commerce<br>Patent and Trademark Office<br><br>Information Disclosure Statement by Applicant | Atty. Docket Number<br><b>CHAN3228/EM</b>   | Serial Number<br><b>10/699,839</b> |
|  | Applicant<br><b>Edward Y. CHANG et. al.</b> |                                    |
|  | Filing Date<br><b>November 4, 2003</b>      | Group<br><b>Unassigned</b>         |

## U.S. Patent Documents

| Examiner Initial | Document Number | Date       | Patentee/Applicant      | Class | Subclass | Filing Date if Appropriate |
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## Foreign Patent Documents

| Examiner Initial | Document Number | Publication Date | Country/Agency | Class | Subclass | Translation |    |
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|                  |                 |                  |                |       |          | Yes         | No |
|                  |                 |                  |                |       |          |             |    |

## Other Documents (Including Author, Title, Date, Pertinent Pages, Place of Publication, Etc.)

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|  | R. D. Bringans et. al., <i>Use of ZnSe as an interlayer for GaAs growth on Si</i> , July 1992, American Institute of Physics, Applied Physics Letters, Vol. 61, No. 2, pp. 195-197.  |
|  | J. Arokia Raj et. al., <i>High-quality GaAs on Si substrate by the epitaxial lift-off technique using SeS<sub>2</sub></i> , December 1999, American Institute of Physics, Applied Physics Letters, Vol. 75, No. 24, pp. 3826-3828.     |
|  | C. Kadow et. al., <i>Subpicosecond carrier dynamics in low-temperature grown GaAs on Si substrates</i> , October 1999, American Institute of Physics, Applied Physics Letters, Vol. 75, No. 17, pp. 2575-2577.                         |
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| Examiner | Date Considered |
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EXAMINER: Initial if citation is considered, whether or not citation is in conformance with MPEP 609; Draw a line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.